Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

FEATURES

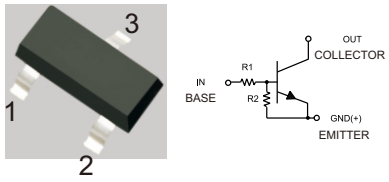
- Reduces board space
- Simplifies Circuit Design
- Reduces Board Space and Component Count

Mechanical Data

- Case: SOT-323
- R_1 = 4.7KΩ (Typ) , R_2 = open

PINNING

PIN	DESCRIPTION
1	BASE
2	EMITTER
3	COLLECTOR



Simplified outline SOT-323 and symbol

MAXIMUM RATINGS (Ta =25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Output current	I_C	100	mA
Power dissipation	P_D	200	mW
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	625	°C/W
Junction temperature	T_J	150	°C
Range of storage temperature	T_{stg}	-55~ +150	°C

ELECTRICAL CHARACTERISTICS(TA = 25°C unless otherwise noted.)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10uA , I_E = 0	50			V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 2mA , I_B = 0	50			V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	I_E = 2mA , I_C = 0	6			V
Collector-Base Cut off Current	I_{CBO}	V_{CB} = 50V , I_E = 0			100	nA
Collector-Emitter Cut off Current	I_{CEO}	V_{CE} = 50V , I_B =0			500	nA
Emitter-Base Cut off Current	I_{EBO}	V_{EB} = 6V , I_C =0			1.9	mA
DC Current Gain	h_{FE}	V_{CE} = 10V , I_C =5mA	160			
Output Voltage (on)	V_{OL}	V_{CE} = 5.0V , V_{BE} = 2.5V , R_L = 1.0KΩ			0.2	V
Output Voltage (off)	V_{OH}	V_{CE} = 5.0V , V_{BE} = 0.25V , R_L = 1.0KΩ	4.9			V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10mA , I_B = 1mA			0.25	V
Input Voltage (off)	$V_{I(off)}$	V_{CE} = 5V , I_C =100μA	0.5			V
Input Voltage (on)	$V_{I(on)}$	V_{CE} = 0.3V , I_C =10mA			1.3	V
Input resistance	R_1		3.3	4.7	6.1	KΩ
Input resistance	R_2		-	-	-	KΩ
Resistance ratio	R_2 / R_1		-	-	-	

Typical Performance Characteristics

Fig 1. VCE(sat) versus IC

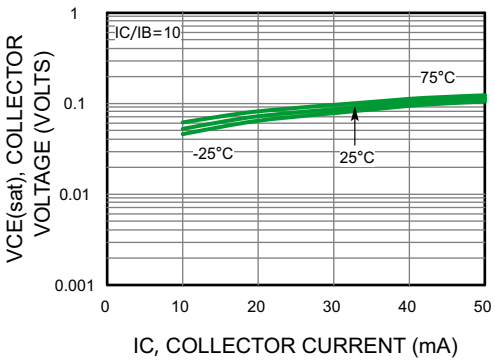


Fig 2. DC Current Gain

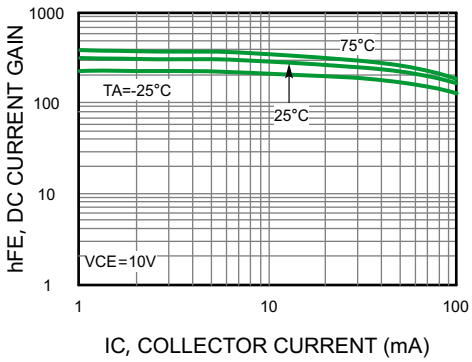


Fig 3. Output Capacitance

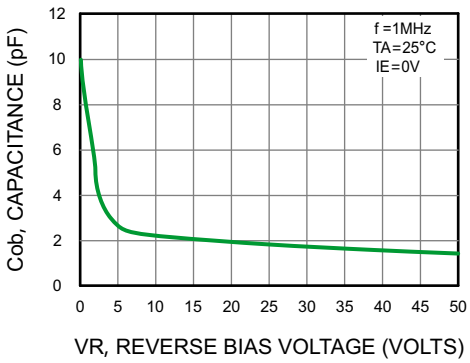


Fig 4. Output Current versus Input Voltage

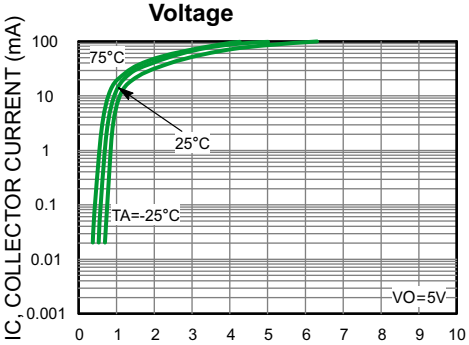
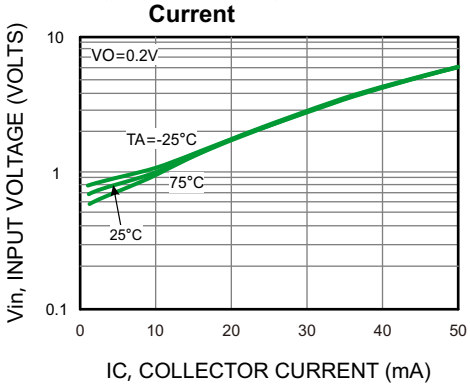
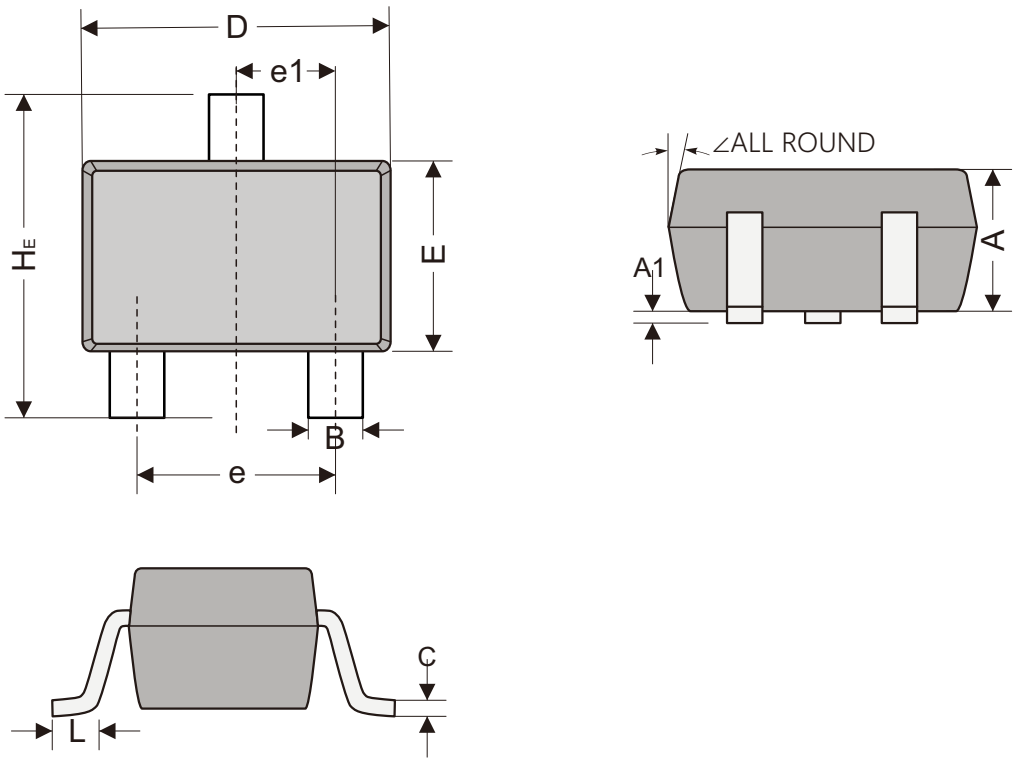


Fig 5. Input Voltage versus Output Current



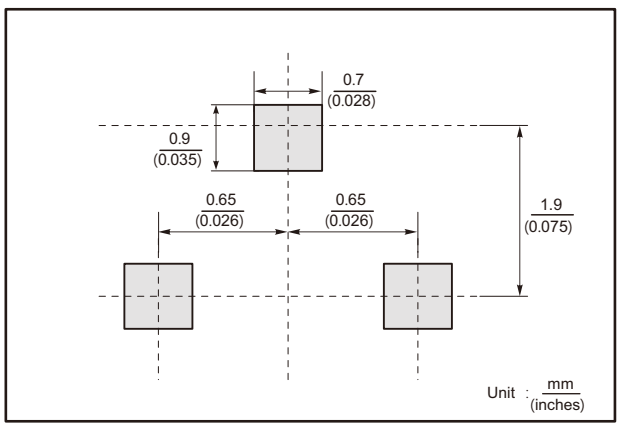
SOT-323 Package Outline Dimensions



SOT-323 mechanical data

UNIT		A	A1	B	C	D	E	e	e1	L	HE
mm	max	1.00	0.10	0.40	0.25	2.20	1.35	1.40	0.65 (BSC)	0.425	2.40
	min	0.80	0.00	0.30	0.10	1.80	1.15	1.20		REF	2.00
mil	max	39.37	3.94	15.75	9.84	86.61	53.15	55.12	25.59 (BSC)	16.73	94.49
	min	31.50	0.00	11.81	3.94	70.87	45.28	47.24		REF	78.74

The recommended mounting pad size



Marking

Type number	Marking code
JDTC143TWG	43T

Important Notice and Disclaimer

Jingdao Microelectronics reserves the right to make changes to this document and its products and specifications at any time without notice.
Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

Jingdao Microelectronics makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, not does Jingdao Microelectronics assume any liability for application assistance or customer product design.

Jingdao Microelectronics does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

No license is granted by implication or otherwise under any intellectual property rights of Jingdao Microelectronics.

Jingdao Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of Jingdao Microelectronics.